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CONSULTATIVE COMMITTEE

SERIES V: DATA COMMUNICATION OVER THE TELEPHONE NETWORK

Interfaces and voice-band modems

ELECTRICAL CHARACTERISTICS FOR UNBALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS

Reedition of CCITT Recommendation V.28 published in the Blue Book, Fascicle VIII.1 (1988)

NOTES

1 CCITT Recommendation V.28 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.28

ELECTRICAL CHARACTERISTICS FOR UNBALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS

(Geneva, 1972; amended at Geneva, 1980, Malaga-Torremolinos, 1984, and at Melbourne, 1988)

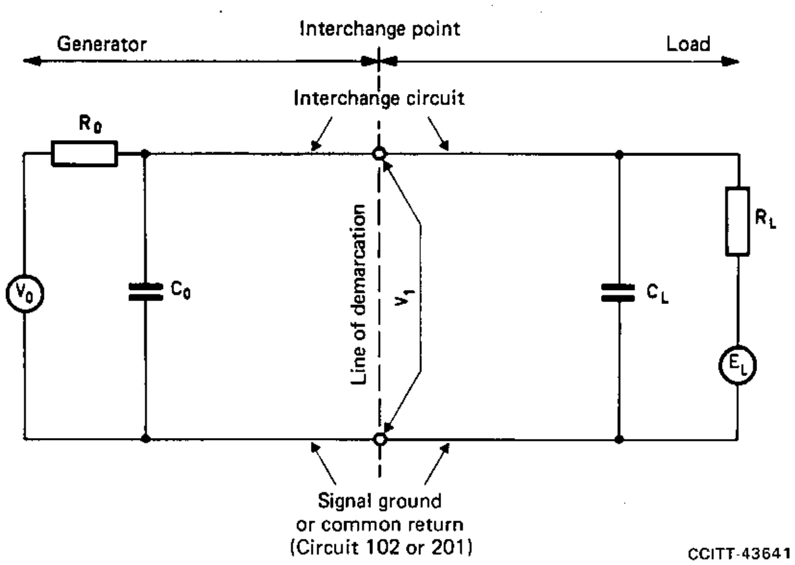
1 Scope

The electrical characteristics specified in this Recommendation apply generally to interchange circuits operating with data signalling rates below the limit of 20 000 bits per second.

2 Interchange equivalent circuit

Figure 1/V.28 shows the interchange equivalent circuit with the electrical parameters, which are defined below.

This equivalent circuit is independent of whether the generator is located in the data circuit-terminating equipment and the load in the data terminal equipment or vice versa.



V_0 is the open-circuit generator voltage.
R_0 is the total effective d.c. resistance associated with the generator, measured at the interchange point.
C_0 is the total effective capacitance associated with the generator, measured at the interchange point.
V_1 is the voltage at the interchange point with respect to signal ground or common return.
C_L is the total effective capacitance associated with the load, measured at the interchange point.
R_L is the total effective d.c. resistance associated with the load, measured at the interchange point.
E_L is the open-circuit load voltage (bias).

FIGURE 1/V.28

Interchange equivalent circuit

The impedance associated with the generator (load) includes any cable impedance on the generator (load) side of the interchange point.

The equipment at both sides of the interface may implement generators as well as receivers in any combination.

For data transmission applications, it is commonly accepted that the interface cabling is provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and is physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 2/V.28.

3 Load

The test conditions for measuring the load impedance are shown in Figure 3/V.28.

The impedance on the load side of an interchange circuit shall have a d.c. resistance (R_L) neither less than 3000 ohms nor more than 7000 ohms. With an applied voltage (E_m), 3 to 15 volts in magnitude, the measured input current (I) shall be within the following limits:

$$I_{\text{min., max.}} = \left| \frac{E_m \pm E_{L\,\text{max.}}}{R_{L\,\text{max., min}}} \right|$$

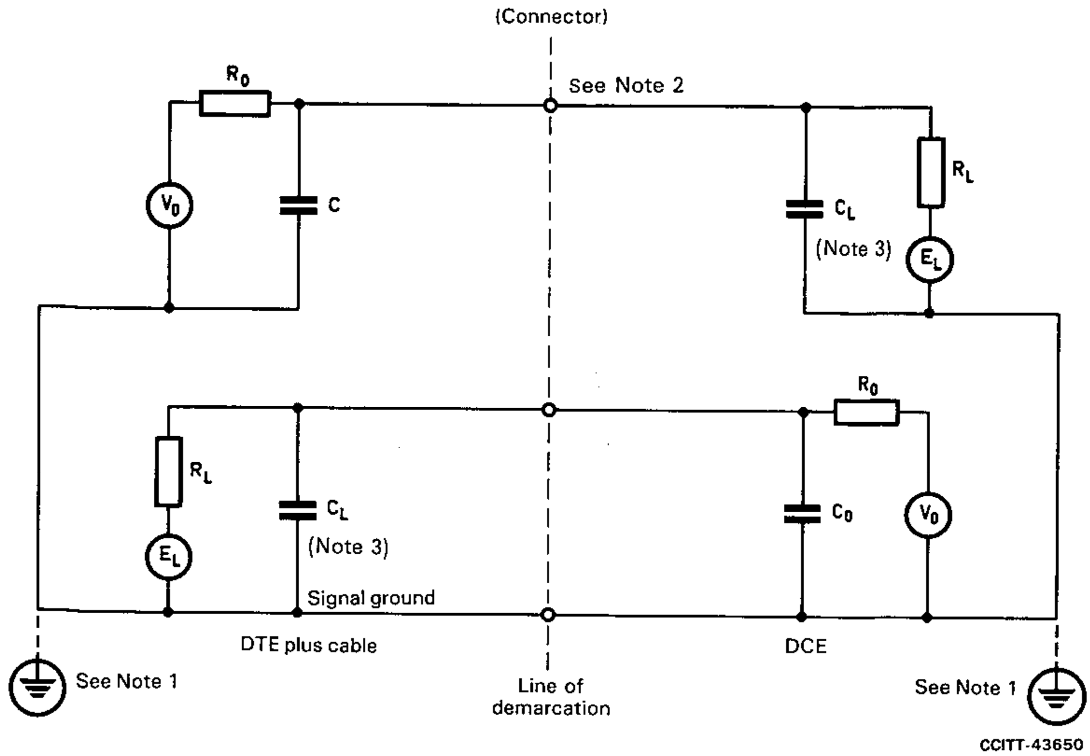
The open-circuit load voltage (E_L) shall not exceed 2 volts.

The effective shunt capacitance (C_L) of the load, measured at the interchange point, shall not exceed 2500 picofarads.

To avoid inducing voltage surges on interchange circuits the reactive component of the load impedance shall not be inductive.

Note – This is subject to further study.

The load on an interchange circuit shall not prejudice continuous operation with any input signals within the voltage limits specified in § 4. below.



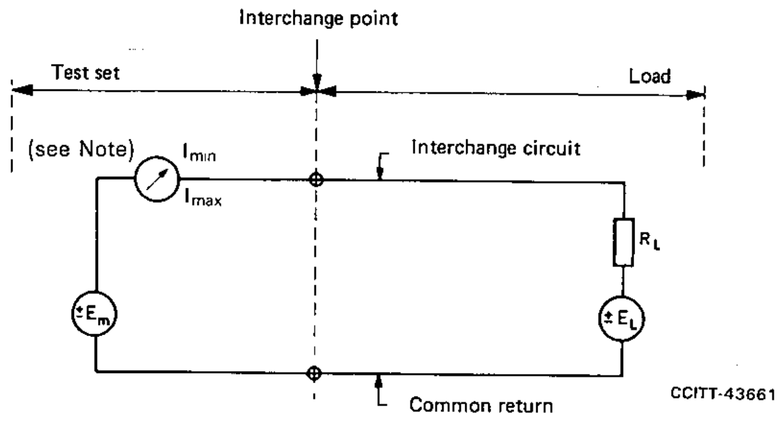
Note 1 – Signal ground may be further connected to external protective ground if national regulations require.

Note 2 – For data transmission over telephone-type facilities, ISO has specified a 25-pin connector and pin assignments in accordance with ISO 2110.

Note 3 – Many existing interchange circuit generators do not provide for meeting the maximum rise time requirement of Recommendation V.28, § 6 when driving a capacitance of greater than 2500 pF, the maximum permitted load capacitance (C_L), which includes the capacitance of the DTE supplied interface cable.

FIGURE 2/V.28

Practical representation of the interface



Note – The internal resistance of the ammeter shall be much less than the load resistance (R_L).

FIGURE 3/V.28

Equivalent test circuit

4 Generator

The generator on an interchange circuit shall withstand an open circuit and a short circuit between itself and any other interchange circuit (including generators and loads) without sustaining damage to itself or its associated equipment.

The open circuit generator voltage (V_0) on any interchange circuit shall not exceed 25 volts in magnitude. The impedance (R_0 and C_0) on the generator side of an interchange circuit is not specified; however, the combination of V_0 and R_0 shall be selected so that a short circuit between any two interchange circuits shall not result in any case in a current in excess of one-half ampere.

Additionally, when the load open-circuit voltage (E_L) is zero, the voltage (V_1) at the interchange point shall not be less than 5 volts and not more than 15 volts in magnitude (either positive or negative polarity), for any load resistance (R_L) in the range between 3000 ohms and 7000 ohms.

The effective shunt capacitance (C_0) at the generator side of an interchange circuit is not specified. However, in addition to any load resistance (R_L) the generator shall be capable of driving all of the capacitance at the generator side (C_0), plus a load capacitance (C_L) of 2500 picofarads.

Note 1 – For test purposes other than specified in this Recommendation (e.g. signal quality measurement), a transmitter test load of 3000 ohms may be used.

Note 2 – Relay or switch contacts may be used to generate signals on an interchange circuit, with appropriate measures to ensure that signals so generated comply with the applicable clauses of § 6 below.

5 Significant levels (V_1)

For data interchange circuits, the signal shall be considered in the binary 1 condition when the voltage (V_1) on the interchange circuit measured at the interchange point is more negative than minus 3 volts. The signal shall be considered in the binary 0 condition when the voltage (V_1) is more positive than plus 3 volts.

For control and timing interchange circuits, the circuit shall be considered ON when the voltage (V_1) on the interchange circuit is more positive than plus 3 volts, and shall be considered OFF when the voltage (V_1) is more negative than minus 3 volts (see Table 1/V.28).

Note – In certain countries, in the case of direct connection to d.c. telegraph-type circuits only, the voltage polarities in Table 1/V.28 may be reversed.

The region between plus 3 volts and minus 3 volts is defined as the transition region. For an exception to this, see § **7** below.

TABLE 1/V.28

Correlation table

$V_1 < -3$ volts	$V_1 > +3$ volts
1	0
OFF	ON

6 Signal characteristics

The following limitations to the characteristics of signals transmitted across the interchange point, exclusive of external interference, shall be met at the interchange point when the interchange circuit is loaded with any receiving circuit which meets the characteristics specified in § 3 above.

These limitations apply to all (data, control and timing) interchange signals unless otherwise specified.

1) All interchange signals entering into the transition region shall proceed through this region to the opposite signal state and shall not re-enter this region until the next significant change of signal condition, except as indicated in 6) below.

2) There shall be no reversal of the direction of voltage change while the signal is in the transition region, except as indicated in 6) below.

3) For control interchange circuits, the time required for the signal to pass through the transition region during a change in state shall not exceed one millisecond.

4) For data and timing interchange circuits, the time required for the signal to pass through the transition region during a change in state shall not exceed 1 millisecond or 3 per cent of the nominal element period on the interchange circuit, whichever is the less.

5) To reduce crosstalk between interchange circuits the maximum instantaneous rate of voltage change will be limited. A provisional limit will be 30 volts per microsecond.

6) When electromechanical devices are used on interchange circuits, points 1) and 2) above do not apply to data interchange circuits.

7 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;

2) receiver not interconnected with a generator;

3) open-circuited interconnecting cable;

4) short-circuited interconnecting cable.

The power-off impedance of the generator side of these circuits shall not be less than 300 ohms when measured with an applied voltage (either positive or negative polarity) not greater than 2 volts in magnitude referenced to signal ground or common return.

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0: No interpretation. A receiver or load does not have detection capability.

Type 1: Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

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